1376P/D922 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In application of: Angela Hui et al.
Serial No.: 09/533,619 Art Unit: 2814
Filed: March 22, 2000 Examiner: W. Louie
For: METHOD AND SYSTEM FOR REDUCING CHARGE GAIN AND CHARGE LOSS WHEN USING AN ARC LAYER INTERLAYER DIELECTIRC FORMATION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION - 37 CFR 1.192)

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on July 15, 2003.

NOTE: "The appellant shall, within 2 months from the date of the notice of appeal under § 1.191 in an application, reissue application, or patent under reexamination, or within the time allowed for response to the action appealed from, if such time is later, file a brief in triplicate." 37 CFR 1.192(a) (emphasis added).

2. STATUS OF APPLICANT

This application is on behalf of

- ☒ other than a small entity
- ☐ small entity

verified statement:

- ☐ attached
- ☐ already filed

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

☐ small entity	$160.00
☒ other than a small entity	$320.00
Appeal Brief fee due	**$320.00**

CERTIFICATE OF MAILING (37 CFR § 1.8)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: 8/29/03

Serena Beller
(Type or print name of person mailing paper)

Serena Beller
(Signature of person mailing paper)

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of § 1.136 for patent applications. 37 CFR 1.191(d). Also see Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply.

(complete (a) or (b) as applicable)

(a) ☐ Applicants petition for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Extension (months)	Fee for other than small entity	Fee for small entity
☐ one month	$ 110.00	$ 55.00
☐ two months	$ 410.00	$ 205.00
☐ three months	$ 930.00	$ 465.00
☐ four months	$ 1,450.00	$ 725.00
Fee		

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

(b) ☒ Applicants believe that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicants have inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief fee $320.00

Extension fee (if any) $0

TOTAL FEE DUE $320.00

6. FEE PAYMENT

☐ Attached is a check in the sum of $____

☒ Charge Account No. 01-0365 (1376P/D922) the sum of $320.00.

A duplicate of this transmittal is attached.

7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum, six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

☒ If any additional extension and/or fee is required, this is a request therefor and to charge Account No. 01-0365 (1376P/D922).

AND/OR

☒ If any additional fee for claims is required, charge Account No. 01-0365 (1376P/D922).

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Hui et al.

Serial No.: 09/533,619

Filed: March 22, 2000

Group Art Unit: 2814

Before the Examiner: Louie, W.

Title: METHOD AND SYSTEM FOR REDUCING CHARGE GAIN AND CHARGE LOSS WHEN USING AN ARC LAYER INTERLAYER DIELECTRIC FORMATION

APPEAL BRIEF

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 29, 2003.

Serena Beller
Signature

Serena Beller
(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-7 are pending in the Application. Claims 8-13 are withdrawn. Claims 1-7 stand rejected.

IV. STATUS OF AMENDMENTS

The Appellants' response to the Office Action, having a mailing date of November 18, 2002, has been considered, but the Examiner indicated that it did not place claims 1-7 in condition for allowance because the Appellants' arguments were deemed unpersuasive.

V. SUMMARY OF INVENTION

A conventional semiconductor device, such as a conventional embedded flash memory, includes several layers of components. Specification, Page 1, Lines 7-8. For example, memory cells in a memory region of the semiconductor device may be in the layer of components on and just above the substrate. Specification, Page 1, Lines 8-10. Components in subsequent layers should be electrically insulated from components in layers above and below except where electrical connection is specifically desired to be made. Specification, Page 1, Lines 10-12. The layer that isolates distinct layers is known as the inter-layer dielectric ("ILD"). Specification, Page 1, Lines 12-13. Electrical connection to lower layers is made using conventional contacts which extend through the ILD. Specification, Page 1, Lines

13-14. The conventional contacts typically include via plugs which extend through via holes in the ILD. Specification, Page 1, Lines 14-15.

In fabricating a conventional embedded flash memory, components, e.g., memory cells, in the lower layer of the semiconductor device may be fabricated followed by providing an ILD on the lower layer to insulate the lower layer from subsequent layers. Specification, Page 1, Lines 16-21.

Typically, contact is made to various portions of the lower layer through the ILD. Specification, Page 2, Line 4. Thus, conventional contacts are fabricated. Specification, Page 2, Line 5. In order to fabricate a conventional contact, a conventional SiON antireflective coating ("ARC") layer of a desired thickness is deposited. Specification, Page 2, Lines 5-6. The desired thickness is typically approximately two hundred to four hundred Angstroms. Specification, Page 2, Lines 7-8. The ARC layer helps to reduce reflections from the ILD layer and other underlying layers when providing a photoresist structure. Specification, Page 2, Lines 8-9. The ARC layer is used because reflections from underlying layers can cause errors in the photoresist structure provided. Specification, Page 2, Lines 9-11. In particular, without the ARC layer of the desired thickness, the critical dimension of structures formed using the photoresist structure may vary widely from the desired dimension. Specification, Page 2, Lines 11-13.

A first photoresist structure is then provided on the conventional ARC layer. Specification, Page 2, Line 14. The first photoresist structure is typically provided by spinning a layer of photoresist onto the ARC layer and using photolithography to develop a pattern, or mask, in the photoresist layer. Specification, Page 2, Lines 15-17. The photoresist structure includes apertures of the desired size over regions of the ILD in which via holes are desired to be etched. Specification, Page 2, Lines 17-18.

Once the first photoresist structure has been provided, the conventional via holes are etched in the ILD. Specification, Page 2, Lines 19-20. The resist structure

is then stripped, typically using a dry oxygen ashing and wet etch. Specification, Page 2, Lines 20-21. Further, residues are cleaned. Specification, Page 2, Line 21. The conventional via holes are filled with a conductive material, forming a conventional via plug, or conventional contact. Specification, Page 2, Lines 21-23. The conventional via plug is typically composed of tungsten (W). Specification, Page 2, Line 23 – Page 3, Line 1. Thus, electrical contact can be made to structures in the lower layer. Specification, Page 3, Line 1. However, excess W outside of the conventional via holes should be removed to provide discrete contacts. Specification, Page 3, Lines 1-2. Furthermore, in order to allow cells in the semiconductor device to be erased using ultraviolet ("UV") light, the ARC layer may need to be removed. Specification, Page 3, Lines 3-4. Thus, the excess W is polished away and the ARC layer is removed using a chemical-mechanical polish ("CMP"). Specification, Page 3, Lines 4-5. The ARC layer is polished away at the end of the W polishing step, typically using an oxide buff. Specification, Page 3, Lines 6-7. Processing of the semiconductor device then continues which typically includes fabricating components for subsequent layers and the ILD layers which separate subsequent layers. Specification, Page 3, Lines 7-9.

Because the ARC layer has been removed, the memory cells in the lower layer can be erased. Specification, Page 3, Lines 19-20. One of ordinary skill in the art will readily understand that the above outlined process may result in charge gain and charge loss issues. Specification, Page 3, lines 21-23. In particular, components in the semiconductor device may unexpectedly gain or lose charge. Specification, Page 3, Line 23 – Specification, Page 4, Line 1. For example, charge on a conventional contact may travel to the memory cell when a user does not desire the memory cell to store charge. Specification, Page 4, Lines 1-3. Similarly, a charge stored on a floating gate of the memory cell may travel to the conventional contact. Specification, Page 4, Lines 3-4. Thus, a charge intentionally stored on the floating gate may bleed away. Specification, Page 4, Lines 4-5. Further, the memory cells

may be subject to unanticipated charge gain and charge loss. Specification, Page 4, Lines 5-6. As a result, the memory cell may not function as desired. Specification, Page 4, Lines 6-7.

The problems outlined above may at least in part be solved in some embodiments by removing the ARC layer without the use of a chemical mechanical polish such as with a plasma etch. Specification, Page 4, Line 23 – Page 5, Line 1. In one embodiment of the present invention, an interlayer dielectric may be provided on a lower layer of the semiconductor device. Specification, Page 4, Lines 14-15. At least a portion of an ARC layer may be provided on the interlayer dielectric. Specification, Page 4, Lines 15-17. A plurality of via holes may be provided in the interlayer dielectric and the ARC layer and the plurality of via holes may be filled with a conductive material. Specification, Page 4, Lines 17-19. The ARC layer may be removed while reducing subsequent undesirable charge gain and subsequent undesirable charge loss resulting from the use of a chemical mechanical polish in removing the ARC layer. Specification, page 4, Lines 19-22.

VI. ISSUES

A. Is claim 1 properly rejected under 35 U.S.C. §102(e) as being unpatentable over Feldner et al. (U.S. Patent No. 6,300,235) (hereinafter "Feldner")?

B. Are claims 2-3 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Feldner in view of Brooks et al. (U.S. Patent No. 5,786,276) (hereinafter "Brooks")?

C. Are claims 4-6 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Feldner in view of Wuu et al. (U.S. Patent No. 6,222,214) (hereinafter "Wuu")?

D. Is claim 7 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Feldner?

VII. GROUPING OF CLAIMS

Claims 1-7 should not be grouped and should be considered separately.

The reasons for these groupings are set forth in Appellants' arguments in Section VIII.

VIII. ARGUMENT

A. Claim 1 is not properly rejected under 35 U.S.C. § 102(e) as being unpatentable over Feldner

The Office Action states that claim 1 is rejected under 35 U.S.C. §102(e) as being anticipated by Feldner. Paper no. 9, page 2. Appellants respectfully traverse this rejection for the reasons stated below.

For a claim to be anticipated over 35 U.S.C. §102, *each and every claim limitation must be found within the cited prior art reference*. M.P.E.P. §2131.

Feldner does not disclose "*removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the ARC layer*" as recited in claim 1. The Examiner asserts that Feldner inherently discloses removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the ARC layer. Paper no. 7, page 3. Appellants respectfully contest the assertion that it is inherently disclosed.

In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, in order for the Examiner to establish inherency, the Examiner must provide extrinsic evidence that must make clear that the missing descriptive matter is

necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Inherency, however, may not be established by probabilities or possibilities. *Id.* The mere fact that a certain thing may result from a given set of circumstances is not sufficient. *Id.* Therefore, the Examiner must support the inherency argument with objective evidence meeting the above requirements. The Examiner has not presented sufficient evidence that the missing descriptive matter is necessarily present in the reference, and that it would be so recognized by persons of ordinary skill. Accordingly, the Examiner has not established that Feldner discloses all the limitations of claim 1.

Further, the Examiner states:

> Applicant argues that Feldner et al. (US 6,300,235) do not disclose 'removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the arc layer.' However, 'reducing subsequent undesirable charge gain and subsequent undesirable charge loss' *is a functional language, which does not carry any patentable weight.* Since applicant does not claim what type of ARC removal process, any removal process other than CMP such as the reactive ion etching would meet the limitation. Therefore, Feldner et al. meet the limitations of claim 1." Paper no. 9, page 6.

Thus, the Examiner asserts that the language "*reducing subsequent undesirable charge gain and subsequent undesirable charge loss*" in claim 1 is functional language and that functional language does not carry any patentable weight. Appellants contest the assertion that simply because functional language is recited in a process claim that the functional language does not carry any patentable weight. There is nothing ineherently wrong with defining some part of an invention in functional terms. M.P.E.P. §2173.05(g). Functional language does not, in and of itself, render a claim improper. *In re Swinehart*, 169 U.S.P.Q. 226, 299 (C.C.P.A. 1971). A functional limitation may be used in association with an element, ingredient or step of a process to define a particular capability or purpose that is served by the

recited element, ingredient or step. M.P.E.P. §2173.05(g). Consequently, the Examiner may not simply ignore such functional language in a process claim. Therefore, the Examiner has not shown that Feldner discloses each and every claim limitation in claim 1. M.P.E.P. § 2131

As a result of the foregoing, Appellants respectfully assert that not each and every claim limitation was found within the cited prior art reference and thus claim 1 is not anticipated by Feldner.

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that only those words are not disclosed in the cited prior art.

B. Claims 2-3 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Feldner in view of Brooks.

The Office Action has further rejected claims 2-3 under 35 U.S.C. § 103(a) as being unpatentable over Feldner in view of Brooks. Paper no. 9, page 4.

1. The Examiner Has Not Provided A *Prima Facie* Case Of Obviousness For Rejecting Claims 2-3.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art references to make the claimed invention. M.P.E.P. §2142. The motivation or suggestion to combine references must come from one of three possible sources: the nature of the problem to be solved, the teaching of the prior art and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 U.S.P.Q.2d. 1453, 1458 (Fed. Cir. 1998). The showings must be clear and particular. *In re* Lee, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617

(Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

> The Examiner states:
>
> > With regard to claims 2 and 3, Feldner et al. disclose utilizing a RIE with C_4F_8 type fluorine containing chemistry etching (col. 6, lines 54-62), ***but do not disclose the plasma etching with CH_3F/O_2 or CHF_3/O_2***. However, Brooks et al. disclose a plasma etching process (Brooks col. 2, lines 50-54) using a mixture of methyl fluoride (CH_3F), carbon tetrafluoride (CF_4) and oxygen (O_2) to remove the ARC (Brooks col. 2, lines 57-64 and table 1A). Brooks et al. teach that it is difficult to etch silicon nitride (Brooks col. 2, lines 31-36) and Brooks et al. introduce the chemical downstream etching which is faster and selectively for nitride (Brooks col. 3, lines 20-23). *Therefore, it would have been obvious to one with ordinary skill in the art to modify Feldner's method with the teaching of Brooks et al. to use CH_3F, CF_4, and O_2 mixture to dry plasma etch the ARC in order to yield faster rate.* Paper no. 9, page 4.

Thus, the Examiner's motivation for modifying *Feldner* with *Brooks* to "*remove the ARC layer using the plasma etch which utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry*," as recited in claims 2 and 3, is that it would have been obvious to one of ordinary skill in the art "*to dry plasma etch the ARC in order to yield faster rate.*" Paper no. 9, page 4.

The Examiner has not established a motivation to combine Feldner with Brooks. In particular, there is no suggestion or motivation in either Feldner or Brooks, or in their combination, or in the knowledge of those ordinarily skilled in the art to combine the teaching of *performing a dual damascene etch through a layer stack disposed above a substrate*, as taught in Feldner, with the teaching of a *chemical downstream etching (CDE) that is selective to silicon nitrides (SiN) over silicon oxides (SiO)*, as taught in Brooks.

Feldner teaches:

> The organic ARC layer 513 may be etched by placing the wafer in an oxide etch chamber where a first etch process known in the art as RIE utilizing N_2 etchant source gas breaks through the organic ARC layer 513 in the areas exposed by the developed photoresist. Col. 6, lines 54-57.

Thus, Feldner teaches etching an ARC layer using a process known in the art as RIE.

Brooks teaches that:

> *As a result of such drawbacks, a number of workers in the field have begun to use dry plasma etching of silicon nitride instead of wet etching.* Dry plasma etching often uses disassociated radicals of fluorine or of other halogens for etching quickly through the otherwise difficult-to-cut silicone nitride material. Col. 2, lines 31-36.

Brooks further teaches that:

> In accordance with a first aspect of the invention, *one or both of the gaseous compounds, CH_3F (methyl fluoride) and CH_2F_2 (ethyl difluoride) are used in combination with CF_4 (carbon tetrafluoride) and O_2 (oxygen) to create a remote plasma.* A downstream output (afterglow) of the plasma is applied to a wafer or other like workpiece that has exposed silicon nitride adjacent to exposed silicon oxide and/or exposed silicon. Col. 2, lines 57-64.

Thus, Brooks teaches dry plasma etching through the otherwise difficult to cut ***silicon nitride material*** using a mixture of CH_3F (methyl fluoride) in combination with CF_4 (carbon tetrafluoride) and O_2 (oxygen). The Examiner does not show why the teaching of *performing a dual damascene etch through a layer stack disposed above a substrate*, as taught in *Feldner*, would be combined with the teaching of a *chemical downstream etching (CDE) that is selective to silicon nitrides (SiN) over silicon oxides (SiO)*, as taught in *Brooks*, from either *the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must submit **objective** evidence and not rely on his own subjective opinion for combining Feldner,

which teaches *performing a dual damascene etch through a layer stack disposed above a substrate*, with Brooks, which teaches *chemical downstream etching (CDE) that is selective to silicon nitrides (SiN) over silicon oxides (SiO).*

As stated above, the Examiner's motivation for modifying Feldner with Brooks to "*remove the ARC layer using the plasma etch which utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry*," as recited in claims 2 and 3, is *to dry plasma etch the ARC in order to yield faster rate.* Paper no. 9, page 4. However, as stated above, Brooks teaches dry plasma etching through the otherwise difficult to cut ***silicon nitride material***. ***Feldner does not teach etching silicon nitride****, but instead teaches etching ARC layer 513.* The Examiner has not shown why Feldner should be modified to use a process to ***etch silicon nitride*** from either *the nature of the problem to be solved, the teachings of the prior art or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Further, the Examiner has not shown why Feldner should be modified with Brooks to use a CH_3F, CF_4 and O_2 mixture to dry plasma etch the ARC in order to yield faster rate from either the *nature of the problem to be solved, the teachings of the prior art or in the knowledge of persons of ordinary skill in the art. Id.* Furthermore, the Examiner has not shown why Feldner should be modified with Brooks to *remove the ARC layer using the plasma etch which utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry* from either *the nature of the problem to be solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. Id.* The Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying Feldner with Brooks to use a silicon nitride etch as taught in Brooks. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying Feldner with Brooks to use a CH_3F, CF_4 and O_2 mixture to dry plasma etch the ARC in order to yield faster rate. *Id.* Further, the Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of

modifying Feldner with Brooks to *remove the ARC layer using a plasma etch where a plasma etch utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry. Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3.

2. Feldner and Brooks, Taken Singly or in Combination, Do Not Teach or Suggest the Limitations of Claims 2-3.

Feldner and Brooks, taken singly or in combination, do not teach or suggest "*removing the ARC layer using the plasma etch*" as recited in claim 2. The Examiner states that Brooks "disclose a plasma etching processing (*Brooks* col. 2, lines 50-54) using a mixture of methyl fluoride (CH_3F), carbon tetrafluoride (CF_4) and oxygen (O_2) to remove the ARC." Paper no. 9, page 4. Instead, as stated above, Brooks teaches:

> *As a result of such drawbacks, a number of workers in the field have begun to use dry plasma etching of silicon nitride instead of wet etching.* Dry plasma etching often uses disassociated radicals of fluorine or of other halogens for etching quickly through the otherwise difficult-to-cut silicone nitride material. Col. 2, lines 31-36.

Brooks further teaches that:

> In *accordance with a first aspect of the invention, one or both of the gaseous compounds, CH_3F (methyl fluoride) and CH_2F_2 (ethyl difluoride) are used in combination with CF_4 (carbon tetrafluoride) and O_2 (oxygen) to create a remote plasma.* A downstream output (afterglow) of the plasma is applied to a wafer or other like workpiece that has exposed silicon nitride adjacent to exposed silicon oxide and/or exposed silicon. Col. 2, lines 57-64.

Brooks further teaches that:

> Wafer backside Helium cooling pressure: 8 Torr. The central recipe point of Table 1A has been found to exhibit *SIN etch rates* of about 2400 A/min or higher and selectively for nitride over nitride of about 60 to 1 or greater. Col. 3, lines 20-23.

Thus, Brooks teaches dry plasma etching *silicon nitride material* using one or both of the gaseous compounds CH_3F and CH_2F_2 in combination with CF_4 and O_2. Hence, Brooks does not teach or suggest *removing an ARC layer using a plasma etch* but instead *teaches etching difficult-to-cut silicon nitride material.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 2. M.P.E.P. §2143.

Furthermore, Feldner and Brooks, taken singly or in combination, do not teach or suggest "wherein the plasma etch further *utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry*" as recited in claim 3. As stated above, the Examiner states that Brooks "disclose a plasma etching processing (*Brooks* col. 2, lines 50-54) using a mixture of methyl fluoride (CH_3F), carbon tetrafluoride (CF_4) and oxygen (O_2) to remove the ARC." Paper no. 9, page 4. Instead, as stated above, Brooks teaches dry plasma etching *silicon nitride material* using one or both of the gaseous compounds CH_3F and CH_2F_2 in combination with CF_4 and O_2. Hence, Brooks does not teach or suggest plasma etch *using a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry.* Instead, Brooks teaches *using one or both of the gaseous compounds CH_3F and CH_2F_2 in combination with CF_4 and O_2.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 3. M.P.E.P. §2143.

As a result of the foregoing, Applicants respectfully assert that since there are numerous claim limitations not taught or suggested in the cited prior art, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-3 in view of the cited prior art. M.P.E.P. §2143.

C. Claims 4-6 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Feldner in view of Wuu.

The Office Action has further rejected claims 4-6 under 35 U.S.C. § 103(a) as being unpatentable over Feldner in view of Wuu. Paper no. 9, pages 4-5.

1. The Examiner Has Not Established A *Prima Facie* Case of Obviousness For Rejecting Claims 4-6

As stated above, a *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142.

The Examiner states:

> With regard to claim 4, Feldner et al. disclose the conductive material used to fill the plurality of via holes (col. 1, lines 40-44), but do not disclose the conductivity material is tungsten. *However, tungsten is a common material used to create a contact plug, such as disclosed in Wuu et al. (Wuu col. 7, lines 12-13). Therefore, it would have been obvious to use tungsten to fill the plurality of via holes.*
>
> With regard to claim 5, Feldner et al. do not disclose the interlayer dielectric is BPTEOS. However, Wuu et al. disclose a method of forming metal contacts in a semiconductor device utilizing BPTEOS as interlayer dielectric layer (Wuu col. 6, lines 32-44). *Wuu et al. teach that BPTEOS is a low flow glass and a good barrier layer (Wuu col. 6, lines 32-44). Therefore, it would have been obvious to one with ordinary skill in the art to modify Feldner's method with the teaching of Wuu to use BPTEOS as dielectric interlayer in order to apply it easily and it is good barrier layer.*
>
> With regard to claim 6, Feldner et al. disclose the device interconnected to form memory cells such as RAM, DRAM, and ROM (col. 4, lines 55-67), but do not disclose the lower layer includes memory cell fabricated on the semiconductor device. *However, it is well known in the art to have memory cell on the lower layer under the interconnects such as disclosed in Wuu et al. forming SRAM cells with the interconnect metal contacts (Wuu fig. 9). Therefore, it would have been obvious to include a plurality of memory cells on the semiconductor layer in Feldner's device.* Paper no. 9, pages 4-5.

The Examiner does not provide any objective motivation for modifying Feldner with Wuu to: (1) "fill the plurality of via holes" with "tungsten," as recited in claim 4; (2)

include an interlayer dielectric that is "BPTEOS," as recited in claim 5; and (3) include a lower layer that "includes a plurality of memory cells and is a first layer fabricated on the semiconductor device," as recited in claim 6. All the Examiner provides is his own subjective opinion which does not amount to the required objective evidence. Further, the Examiner's motivation for modifying Feldner with Wuu to provide an interlayer dielectric that is BPTEOS, as recited in claim 5, is "in order to apply it easily and it is good barrier layer." Paper no. 9, page 5. Again, this is the Examiner's subjective opinion and not objective evidence.

There is no motivation to combine Feldner with Wuu. In particular, there is no suggestion or motivation in either Feldner or Wuu, or in their combination, or in the knowledge of those ordinarily skilled in the art to combine the teaching of *performing a dual damascene etch through a layer stack disposed above a substrate*, as taught in Feldner, with the teaching of *fabricating a novel plug structure for low resistance ohmic stacked contacts and at the same time forming metal contacts to devices on a SRAM cell*, as taught in Wuu. As stated above, Feldner teaches performing a dual damascene etch through a layer stack disposed above a substrate.

Wuu teaches:

> [a] *method for fabricating a novel plug structure for low resistance ohmic stacked contacts and at the same time forming metal contacts to devices on a SRAM cell.* Abstract.

The Examiner has not objectively shown why the teaching of *performing a dual damascene etch through a layer stack disposed above a substrate*, as taught in Feldner, would be combined with the teaching of *fabricating a novel plug structure for low resistance ohmic stacked contacts and at the same time forming metal contacts to devices on a SRAM cell*, as taught in Wuu, from either *the nature of the problem to be solved, the teaching in the prior art or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must submit **objective evidence** for combining Feldner with Wuu.

As stated above, the Examiner does not provide any objective motivation for modifying Feldner with Wuu to "fill the plurality of via holes" with "tungsten," as recited in claim 4. Paper no. 9, page 4. The Examiner has not objectively shown why Feldner should be modified to fill the via holes with tungsten from either *the nature of the problem to be solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Instead, the Examiner states that "tungsten is a common material used to create a contact plug, such as disclosed in Wuu et al. (Wuu, Col. 7, lines 12-13)." Paper No. 9, page 4. The Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying Feldner to fill via holes with tungsten. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Furthermore, as stated above, the Examiner's motivation for modifying Feldner with Wuu to provide an interlayer dielectric that is "BPTEOS," as recited in claim 5, is "in order to apply it easily and it is good barrier layer." Paper No. 9, page 5. Wuu teaches that:

> [a] third insulating layer 22 is deposited over the patterned layer 18, as also shown in FIG. 7. Preferably the insulating layer is composed of a low flow glass to provide a *leveling effect for planarizing the surface.* For example, *layer 22 can be deposited by low pressure chemical vapor deposition (LPCVD) reactor by decomposing a tetraethosiloxane (TEOS) while introducing dopants such as phosphine (PH_3) and diborane(6) (B_2H_6) to form the BPTEOS glass.* The glass is then annealed for about between 15 to 60 minutes at a temperature of between about 800 to 900° C to level the glass layer 22. The *layer also serves as a barrier layer to sodium (Na) contamination.* Col. 6, lines 32-44.

Hence, ***Wuu*** **teaches depositing layer 22 to serve as a leveling effect for planarizing the surface and a barrier layer to sodium (Na) contamination**. The Examiner has not objectively shown why Feldner should be modified with Wuu *to deposit a layer that serves as a leveling effect for planarizing the surface and a barrier layer to sodium contamination* from either *the nature of the problem to be*

solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. In re Rouffet, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Further, the Examiner has not objectively shown why Feldner should be modified with Wuu to *provide an interlayer dielectric on the lower level that is BPTEOS* from either *the nature of the problem to be solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. Id.* The Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying Feldner *to deposit a layer that serves as a leveling effect for planarizing the surface and a barrier layer to sodium contamination. In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Further, the Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying Feldner to *provide an interlayer dielectric on the lower level that is BPTEOS. Id.*

Further, as stated above, the Examiner does not provide any objective motivation for modifying Feldner with Wuu to include a lower layer that "includes a plurality of memory cells and is a first layer fabricated on the semiconductor device," as recited in claim 6. Paper no. 9, page 5. The Examiner has not objectively shown why Feldner should be modified to include a lower layer that includes a plurality of memory cells and is a first layer fabricated on the semiconductor device from either *the nature of the problem to be solved, the teaching of the prior art, or the knowledge of persons of ordinary skill in the art. In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). Instead, the Examiner expresses his subjective opinion that "it is well known in the art to have memory cell on the lower layer under the interconnects such as disclosed in Wuu et al. forming SRAM cells with the interconnect metal contacts (Wuu fig. 9). Therefore, it would have been obvious to include a plurality of memory cells on the semiconductor layer in Feldner's device." Paper No. 9, page 5. The Examiner must submit **objective evidence** and not rely on his own subjective opinion in support of modifying Feldner to include a lower layer that includes a plurality of

memory cells and is a first layer fabricated on the semiconductor device. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Therefore, for at least the reasons stated above, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6.

2. Feldner and Wuu, Taken Singly or in Combination, do not Teach or Suggest the Limitations of Claims 5 and 6

Feldner and Wuu, taken singly or in combination, do not teach or suggest "*wherein the interlayer dielectric is BPTEOS*" as recited in claim 5. The Examiner admits that "Feldner et al. do not disclose the interlayer dielectric is BPTEOS," but submits that: "Wuu et al. disclose a method of forming metal contacts in a semiconductor device utilizing BPTEOS as interlayer dielectric layer (Wuu col. 6, lines 32-44). Wuu et al. teach that BPTEOS is a low flow glass and a good barrier layer (Wuu col. 6, lines 32-44)." Paper No. 9, pages 4-5. Instead, Wuu teaches:

> [a] third insulating layer 22 is deposited over the patterned layer 18, as also shown in FIG. 7. Preferably the insulating layer is composed of a low flow glass *to provide a leveling effect for planarizing the surface*. For example, layer 22 can be deposited by low pressure chemical vapor deposition (LPCVD) reactor by decomposing a tetraethosiloxane (TEOS) while introducing dopants such as phosphine (PH_3) and diborane(6) (B_2H_6) to form the BPTEOS glass. The glass is then annealed for about between 15 to 60 minutes at a temperature of between about 800 to 900° C to level the glass layer 22. The *layer also serves as a barrier layer to sodium (Na) contamination.* Col. 6, lines 32-44.

Thus, Wuu teaches a third insulating layer 22 (Figure 7 of Wuu) on top of patterned layer 18 (Figure 7 of Wuu) and second insulating layer 16 (Figure 7 of Wuu) where the third insulating layer 22 (BPTEOS glass) may be used to provide a leveling effect for planarizing the surface and to *serve as a barrier layer to sodium contamination.* This language does not teach or suggest that *layer 22 is an interlayer* dielectric. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 5. M.P.E.P. §2143.

Feldner and Wuu, taken singly or in combination, do not teach or suggest "wherein the lower layer includes a *plurality of memory cells* and is a *first layer fabricated on the semiconductor device*" as recited in claim 6. The Examiner directs Appellants' attention to Figure 9 of Wuu as teaching the above-cited claim limitation. Paper no. 9, page 5. Instead, Wuu teaches:

> Referring now to FIG. 9, The novel plug structure is completed by depositing a metal layer 24 to conformally fill the openings 6 and 7 and thereby making an electrical contact between the P+ and N+ layers 14 and 18 in opening 6 and simultaneously making electrical contact to the terminals of the other devices on the substrate in openings 7. The metal layer 24 is then etched back to form the electrically isolated conductive plugs 24 in each contact opening, as shown in FIG. 9. The conductive plugs 24 are preferably composed of a refractory metal, such as tungsten (W), which also functions as a barrier layer to metal penetration from the first metal layer into the silicon contacts on the substrate. The tungsten can be deposited by several methods, such as CVD, physical evaporation, sputtering and the likes, but is preferably accomplished by using CVD and the thermal decomposition of tungsten hexafluoride (WF_6). *FIG. 9 shows the SRAM completed up to the first level metal 26*. For example, an aluminium layer 26 can be deposited and then patterned by photoresist masking an plasma etching to form the first metal interconnect level.
>
> To *simplify the description of the invention FIGS. 6 through 9 show the formation of only one electrical connection between the drain (node Q1FIG. 1) of the first TFT having gate electrode G1 to the gate G2 of the second TFT.* However, *it should be noted that during the processing a second connection is made from the drain (node Q2FIG. 1) of the second TFT to the gate electrode GI of the first TFT.* Both connections are made through stacked contacts between the P^+ and N^+ layers 18 and 14 using metal plugs that electrically short the P^+/N^+ junction and provide a very low resistance ohmic contact, which is a significant improvement over the stacked contacts of the prior art of FIGS. 2 through 5. Column 7, lines 4-36.

Thus, Wuu teaches forming gate electrodes G1 and G2 on insulating layer 12 which is formed on semiconductor 10 as illustrated in Figure 9. Gate electrodes G1 and G2 are not memory cells. Instead, Figure 9 is a diagram of a portion of a memory cell

(SRAM cell). Hence, Wuu does not teach or suggest a lower layer that includes *a plurality of memory cells*. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 6. M.P.E.P. §2143.

As a result of the foregoing, Applicants respectfully assert that since there are numerous claim limitations not taught or suggested in the cited prior art, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6 in view of the cited prior art. M.P.E.P. §2143.

D. Claim 7 is not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Feldner.

Feldner does not teach or suggest "*providing a chemical mechanical polish of the conductive material*" as recited in claim 7. The Examiner states:

> With regard to claim 7, *Feldner et al.* disclose the trench is filled with metal, which is then polished (col. 1, lines 29-32), but *do not disclose a chemical mechanical polish process is used. However, the chemical mechanical polish process is well known in the art. Therefore, it would have been obvious to use chemical mechanical polish process to polish the metal.* Paper no. 9, page 3.
>
> Applicant argues that CMP process applies to a conductive layer in claim 7 is not a well-known process. *However, CMP applies to a conductive layer is very common such as disclosed in Tsou et al. (U.S. 6,265,305), Lee (US 6,300,672), Avanzino et al. (US 6,410,443), Hui et al. (US 6,506,683), and Chen (US 6,509,278). Therefore, CMP applied on a conductive layer is a well-known process.* Paper no. 9, page 6.

The Examiner has not submitted **objective evidence** in support of modifying Feldner to provide a chemical mechanical polish of the conductive material. *In re Lee* 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Instead, the Examiner lists some patents that teach a chemical mechanical polish but does not provide any **objective evidence** for combining Feldner with any of these patents listed by the Examiner. *Id.* Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claim 7. M.P.E.P. §2143.

E. Conclusion Regarding 35 U.S.C. §103 Rejections.

As a result of the foregoing, Appellants respectfully assert that since there are numerous claim limitations not taught or suggested in the cited prior, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-7 in view of the cited prior art. M.P.E.P. §2143.

It is noted that words are italicized only for emphasis. Words that are italicized are not meant to imply that only those words are not taught or suggested in the cited prior art.

IX. CONCLUSION

For the reasons noted above, the rejections of claims 1-7 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-7.

Respectfully submitted,

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APPENDIX

1. A method for insulating a lower layer of a semiconductor device from an upper layer of the semiconductor device comprising the sequential steps of:

(a) providing an interlayer dielectric on the lower layer;

(b) providing an antireflective coating (ARC) layer, at least a portion of the ARC layer being on the interlayer dielectric;

(c) providing a plurality of via holes in the interlayer dielectric and the ARC layer;

(d) filling the plurality of via holes with a conductive material; and

(e) removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the ARC layer.

2. The method of claim 1 wherein the ARC layer removing step (e) further includes the steps of:

(e1) removing the ARC layer using a plasma etch.

3 The method of claim 2 wherein the plasma etch further utilizes a CH_3F/O_2 chemistry or a CHF_3/O_2 chemistry.

4. The method of claim 1 wherein the conductive material used to fill the plurality of via holes is W.

5. The method of claim 1 wherein the interlayer dielectric is BPTEOS.

6. The method of claim 1 wherein the lower layer includes a plurality of memory cells and is a first layer fabricated on the semiconductor device.

7. The method of claim 1 further comprising the step of:

(f) providing a chemical mechanical polish of the conductive material.